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Attorney Docket No.: CIS0069US

November 3, 2006

MAIL STOP APPEAL BRIEF - PATENTS
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Re:	Inventors:	Andrew J. Thurston	
	Assignee:	Cisco Technology, Inc.	
	Title:	BCH FORWARD ERROR CORRECTION DECODER	
	Application No.:	09/822,~~590~~ 950	
	Examiner:	Dipakkumar B. Gandhi	Filed: March 30, 2001
	Attorney Docket No.:	CIS0069US	Group Art Unit: 2138

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

(1) Return Receipt Postcard;
(2) This Transmittal Letter (1 page) *(in duplicate)*; and
(3) Appeal Brief (28 pages).

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☒	Please charge our Deposit Account No. 502306 in the amount of	$	500.00
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Brenna A Brock 11/3/2006
Attorney for Appellant Date of Signature

Respectfully submitted,

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Andrew J. Thurston		
Assignee:	Cisco Technology, Inc.		
Title:	BCH FORWARD ERROR CORRECTION DECODER		
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Docket No.:	CIS0069US	Confirmation No.:	6592

Austin, Texas
November 3, 2006

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APPEAL BRIEF

Dear Sir:

This brief is submitted in support of the Notice of Appeal dated September 6, 2006, by Appellant to the Board of Patent Appeals and Interferences from the final rejection of claims 1-8, 10-29, 31-37, and 48-55. A Notice of Panel Decision from Pre-Appeal Brief Review was mailed on September 27, 2006. The Notice of Appeal was filed on August 31, 2006 and received by the United States Patent and Trademark Office on September 6, 2006. Accordingly, this brief is timely submitted within the two-month period, ending on November 6, 2006, after the Notice of Appeal.

Please charge deposit account No. 502306 for the fee of $500.00 associated with this appeal brief. Please charge this deposit account for any additional sums which may be required to be paid as part of this appeal.

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REAL PARTY IN INTEREST

The real party in interest on this appeal is the Assignee, Cisco Technology, Inc.

RELATED APPEALS AND INTERFERENCES

None

STATUS OF CLAIMS

Claims 1-29 and 31-55 are pending in the application.

Claims 1-8, 10-29, 31-37, and 48-55 stand rejected.

Claim 9 is objected to as being dependent upon a rejected base claim.

Claim 30 has been canceled.

Claims 38-47 have been allowed.

Appellant appeals the rejections of claims 1-8, 10-29, 31-37, and 48-55.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection of June 1, 2006.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent claim 1 sets forth a method of decoding an error-correction code in a data signal. The method involves receiving the data signal at a decoding unit. *See, e.g.,* Specification, p. 32, lines 8-10 and elements 52 of FIG. 5. A plurality of syndromes associated with the received data signal are then computed, using the decoding unit. *See, e.g.,* Specification, p. 32, lines 8-21. An error polynomial is then extracted from the data signal. Extracting the error polynomial comprises generating a plurality of minimum-degree polynomials based on no more than six equations having no more than two branch decisions. *Id.* at p. 32, lines 27-28 and p. 33, lines 6-24, where σ^i are the minimum-degree polynomials. Errors within the data signal are then located using the error polynomial. *Id.* at p. 36, lines 10-26.

Independent claim 13 involves a method of determining an error polynomial for decoding a Bose-Chaudhuri-Hocquenghem (BCH) code. The method computes a plurality of syndromes associated with a data signal having a BCH code embedded therein. *See, e.g.,* Specification, p. 32, lines 8-21. The syndromes are fed to a plurality of Galois field multiply accumulators. *See, e.g.,* GFUs 0-3 of FIG. 12 and Specification, p. 34, line 7 through p. 35, line 5 and p. 36, lines 4-5. A plurality of minimum-degree polynomials associated with the BCH code are then calculated, using the Galois field multiply accumulators. *See, e.g.,* Specification, p. 34, line 17 through p. 34, line 13. An error polynomial, which is based on the minimum-degree polynomials, is then generated. *See, e.g.,* Specification, p. 33, line 28 through p. 34, line 1 and p. 35, lines 15-18. The calculating of the minimum degree polynomials and the generating of the error polynomial are performed in no more than 12 clock cycles. *See, e.g.,* Specification, p. 34, line 11 through p. 35, line 15.

Independent claim 25 describes a circuit for generating an error polynomial of a Bose-Chaudhuri-Hocquenghem (BCH) code. *See, e.g.,* FIG. 12. The circuit includes a plurality of syndrome inputs as well as a plurality of Galois field multiply accumulators. *See, e.g.,* GFUs 0-3 of FIG. 12 and p. 36, lines 4-5. The circuit also includes means for

using said Galois field multiply accumulators to generate an error polynomial by generating a plurality of minimum-degree polynomials based on values provided at the syndrome inputs, by executing no more than six equations with two branch decisions. *See, e.g.,* Epoly state machine of FIG. 12 and Specification, p. 34, line 7 through p. 35, line 15.

Independent claim 48 sets forth an OC-192 input/output card. *See, e.g.,* card 10 of FIG. 1. The OC-192 input/output card includes four OC-48 processors (*see, e.g.,* processors 14 of FIG. 1) as well as an OC-192 front-end application-specific integrated circuit (ASIC) (*see, e.g.,* ASIC 12 of FIG. 1) connected to the four OC-48 processors. The OC-192 front-end ASIC has means for de-interleaving an OC-192 signal to create four OC-48 signals. Specification, p. 10, lines 21-23 and p. 10, line 28. The OC-192 front-end ASIC also includes means for decoding error-correction codes embedded in each of the four OC-48 signals. *See, e.g.,* receive module 16 of FIG. 3 and Specification, p. 11, lines 24-28. The decoding means including means for generating an error polynomial associated with a given one of the error-correction codes in no more than 12 clock cycles, wherein said decoding means uses a non-iterative algorithm to generate the error polynomial based on a plurality of minimum-degree polynomials. *See, e.g.,* FIG. 12 and Specification, p. 34, line 7 through p. 35, line 15.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Whether claim 1 is unpatentable under 35 U.S.C. §112, second paragraph, as being indefinite.

II. Whether claim 1 is unpatentable under 35 U.S.C. §103(a) over Oh et al, U.S. Patent No. 5,583,499 (hereinafter referred to as "Oh") in view of Kraft, U.S. Patent No. 5,343,481 (hereinafter referred to as "Kraft"). Dependent claims 2-8, 10-12, and 55 depend from claim 1 and are grouped with claim 1 for purposes of this appeal. The features of independent claim 25 are similar to those of claim 1, and thus claim 25 and its dependent claims 26-29 and 31-37 are grouped with claim 1 for purposes of this appeal.

III. Whether claim 13 is unpatentable under 35 U.S.C. §103(a) over Oh in view of Kraft. Dependent claims 14-24 depend from claim 13 and are grouped with claim 13 for purposes of this appeal.

IV. Whether claim 48 is unpatentable under 35 U.S.C. § 103(a) over Alvarez et al., U.S. Publication No. 2002/0165962 A1 (hereinafter referred to as "Alvarez") in view of Kraft. Dependent claims 49-54 depend from claim 48 and are grouped with claim 48 for purposes of this appeal.

ARGUMENT

I. Whether claim 1 is unpatentable under 35 U.S.C. §112, second paragraph, as being indefinite.

Claim 1 is currently rejected under 35 U.S.C. §112, second paragraph, as being indefinite, for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, as indicated in the Final Office Action mailed June 1, 2006 (hereinafter referred to as "FOA"). The FOA states: "'the extracting comprises generating a plurality of minimum-degree polynomials based on no more than six equations having no more than two branch decisions' does not describe the features of the invention." FOA, p. 3.

The initial version of the §112 rejection of claim 1 was presented on p. 2 of the Non-Final Office Action mailed June 17, 2005. In the June 17, 2005 Non-Final Office Action, the Examiner rejected claim 1 as being indefinite, stating that the claim language "'no more than six equations having no more than two branch decisions' does not clearly mention how many equations are used in the decoding and number of equations does not describe the features of the invention." On pp. 12-13 of Appellant's response, mailed September 19, 2005, Appellant noted that "the claim makes it clear that no more than six equations (i.e., six equations or less) are used to generate the minimum-degree polynomials. Accordingly, Applicant has clearly set forth a range for the number of equations that are used to generate the minimum-degree polynomials." In the same section of the September 19, 2005 response, Appellant also noted that, by "clearly setting forth the maximum number of equations and branch decisions used to generate the minimum-degree polynomials, the claim clearly describes one particular feature of the invention."

On p. 2 the Non-Final Office Action mailed December 14, 2005 (hereinafter referred to as "NFOA"), the Examiner revised the language of the rejection, stating simply: "the extracting comprises generating a plurality of minimum-degree polynomials based on no more than six equations having no more than two branch decisions' does not describe the features of the invention." In response to this new version of the §112

rejection, Appellant again noted the claims clearly described one particular feature of the invention. On pp. 11-12 of the Response mailed March 14, 2006, Appellant further noted: "[t]he meanings of the terms "equations" and "branch decisions" are clear, as is the language specifying the maximum number of each."

The Examiner restated the same version of the §112 rejection in the FOA. In response to the Appellant's arguments presented in the March 14, 2006 response, the Examiner simply states:

> The Examiner disagrees and would like to mention that claim 1 fails to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 1 does not describe the features of the invention. Hence the claim 1 is rejected under 35 U.S.C. §112 as being indefinite. FOA, p. 2, Response to Amendment.

In the current version of the §112 rejection, the Examiner provides no support for the assertion that the claim language "does not describe the features of the invention." The Examiner appears to be using form paragraph 7.34.01 to reject claim 1. Appellants note that MPEP §706.03(d) provides instructions for the use of this form paragraph. These instructions state:

> This form paragraph should be followed by one or more of the following form paragraphs 7.34.02 - 7.34.11, as applicable. If none of these form paragraphs are appropriate, a full explanation of the deficiency of the claims should be supplied. Whenever possible, identify the particular term(s) or limitation(s) which render the claim(s) indefinite and state why such term or limitation renders the claim indefinite. If the scope of the claimed subject matter can be determined by one having ordinary skill in the art, a rejection using this form paragraph would not be appropriate.

In the §112 rejection of claim 1, the Examiner has neither set forth one of form paragraphs 7.34.02-7.34.11 nor supplied any explanation of the deficiency of the claims. For example, the Examiner has not pointed to any statement by the Appellant indicating that the invention differs from what is defined in claim 1. Instead, the Examiner has simply presented the broad assertion that the claim language "does not describe the features of the invention." Accordingly, Appellant respectfully submits that the Examiner has not presented the proper evidence needed to establish a basis for the §112

rejection of claim 1.

Appellant further asserts that claim 1 fully complies with the requirements of 35 U.S.C. §112, second paragraph. Appellants are their own lexicographers and, as such, are free to use "functional language, alternative expressions, negative limitations, or any style of expression or format of claim which makes clear the boundaries of the subject matter for which protection is sought." MPEP §2173.01. In claim 1, Appellant has set forth the scope of the claim by specifying the maximum number of equations and branch decisions that can be used to generate the minimum degree polynomials. The language of claim 1 makes it clear that no more than six equations (i.e., six equations or less) are used to generate the minimum-degree polynomials. The meanings of the terms "equations" and "branch decisions" are clear, as is the language specifying the maximum number of each.

By clearly setting forth the maximum number of equations and branch decisions used to generate the minimum-degree polynomials, the claim clearly describes one particular feature of the invention. Furthermore, claim 1 sets forth the subject matter that Appellant regards as the invention using claim language that is clear to one of ordinary skill in the art. Accordingly, claim 1 satisfies the requirements of §112, second paragraph. As such, Appellant respectfully requests the withdrawal of this rejection.

In the telephone interview of March 13, 2006, Examiner Gandhi stated that the portion of claim 1 reciting "no more than six equations having no more than two branch decisions" was the particular language that did not describe the features of the invention. Examiner Gandhi contrasted claim 1 with claim 9 (which explicitly sets forth one set of equations that can be used to generate an error locator polynomial), stating that claim 9 was an example of a claim that did set forth the features of the invention.

By specifying claim 9 as an example of a claim that does set forth the features of the invention, the Examiner appears to be implying that claim 1 is indefinite simply because claim 1 has greater breadth than claim 9. However, claim breadth is not to be equated with indefiniteness. "If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the invention to be of a scope different from that defined in the claims, then the claims comply with 35

U.S.C. §112, second paragraph." MPEP §2173.94, citing *In re Miller*, 441 F.2d 689, 179 USPQ 597 (CCPA 1971). Accordingly, since the scope of claim 1 is clear (for the reasons set forth above), Appellant asserts that claim 1 is not indefinite merely because it has greater breadth than claim 9.

II. Whether claim 1 is unpatentable under 35 U.S.C. §103(a) over Oh in view of Kraft

Claim 1 stands rejected under 35 U.S.C. §103(a), as being unpatentable over Oh in view of Kraft, as indicated on p. 4 the FOA. Claim 1 recites: extracting an error polynomial from the data signal, wherein the extracting comprises generating a plurality of minimum-degree polynomials based on no more than six equations having no more than two branch decisions."

The rejection of claim 1 relies on lines 2-7 and 33-57 of col. 6 of Kraft to teach this feature of claim 1. NFOA, p. 3, FOA p. 2. In particular, p. 3 of NFOA states:

> Kraft in an analogous art teaches that the binary tree of FIG. 2... code vector (fig. 1, 2, col. 6, lines 2-7, Kraft). Kraft also teaches that the control bits... FIG. 2 occurs (fig. 2, col. 6, lines 33-57, Kraft). (ellipses present in the original)

Similarly, p. 2 of FOA states:

> Kraft teaches that the binary tree of FIG. 2... code vector (fig. 1, 2, col. 6, lines 2-7, Kraft). Kraft also teaches that the control bits... FIG. 2 occurs (fig. 2, col. 6, lines 33-57, Kraft). Hence Kraft teaches generating a plurality of minimum-degree polynomials based on no more than six equations having no more than two branch decisions as mentioned in claim 1. (ellipses present in the original)

The cited portions of Kraft recite:

> The binary tree of FIG. 2 represents the essence of the invention and is traversed by decision means 6 of FIG. 1. The traversal of this decision tree leads to the correct coefficients of the error-location polynomial for the current received code vector. Kraft, col. 6, lines 2-7.
>
> The tree decision variables a 23, b 24, and c 25 are generated by the calculation means 4 in FIG. 1. The control bits cause the polynomial generator 8 of FIG. 1 to make one of the the [sic] following choices as to

the error-location polynomial:

$el1$: $\sigma(x) = 1$

$el3$: $\sigma(x) = 1 + S_3x^3$

$el4$: $\sigma(x) = 1 + e_1x^2 + S_3x^3$

$el5$: $\sigma(x) = 1 + S_1x$

$el7$: $\sigma(x) = 1S_1x + e_2x^2$

$el8$: $\sigma(x) = 1 + S_1x + e_3x^2 + e_4x^3$

where:

$e1 = S_5S_3^{-1}$

$e2 = aS_1^{-1}$

$e3 = ca^{-1} + aS_1^{-1}$

$e4 = ca^{-1}S_1$

> The error condition 51 in FIG. 2 occurs when a received codeword has been corrupted by channel noise with more than three errors. In other words, an error has occurred that is beyond the capability of a three-error correcting BCH code to correct. Kraft, col. 6, lines 33-57.

Kraft describes how an error location polynomial can be found by calculating tree decision variables from the syndromes, and then using the tree decision variables and the syndromes to traverse a binary decision tree. The traversal of the binary decision tree leads to one of the temporary control bits *el*1-*el*8. The selected temporary control bit identifies a respective one of different potential error location polynomials quoted above. The identified one of the polynomials is then selected as the error location polynomial. Kraft, col. 5, line 49 - col. 6, line 36.

The cited art does not teach or suggest "generating a plurality of minimum-degree polynomials"

Appellant respectfully submits that Kraft does not teach or suggest extracting an error polynomial from the data signal, wherein the extracting comprises generating a plurality of minimum-degree polynomials, as recited in claim 1. While Kraft's disclosure

does show several polynomials (each identified by a respective one of temporary control bits *el*1-*el*8) in lines 37-47 of col. 6, multiple ones of these polynomials are not generated in the process of extracting an error polynomial. Instead, a single one of those polynomials is selected as the error locator polynomial, based on which temporary control bit is identified by the traversal of the binary decision tree. Accordingly, Kraft does not teach or suggest generating a plurality of minimum-degree polynomials, as recited in claim 1.

Oh teaches a decoding system that calculates an error locator polynomial using an iterative technique. Oh, Abstract. As noted by the Examiner on p. 3 of NFOA, Oh does not teach or suggest "wherein the extracting comprises generating a plurality of minimum-degree polynomials." Thus, Oh, both alone and in combination with Kraft, also fails to teach or suggest the quoted feature of claim 1. Accordingly, for at least the foregoing reasons, the cited art fails to teach or suggest "generating a plurality of minimum-degree polynomials," as recited in claim 1.

The cited art does not teach or suggest "no more than two branch decisions"

Furthermore, the cited portions of Kraft do not teach or suggest "generating a plurality of minimum-degree polynomials based on no more than six equations having no more than two branch decisions," as recited in claim 1. As shown in FIG. 2 of Kraft, traversal of the binary decision tree, which is used to select an error locator polynomial, involves three branch decisions. One decision occurs at element 13, another decision occurs at either element 12 or 23, and a final decision occurs at one of elements 14, 24, or 25. Kraft states:

> [T]he tree is traversed starting at its root 78 by first examining the syndrome component S_1 13. If this component is 0, a decision is made to go to the left; if not, a decision is made to go to the right. Thus at the second level of the tree either S_3 12 or the tree decision variable a 23 must be examined depending upon which side of the tree the first level decision led to... [E]ither the syndrome component S_5 14 or one of the tree decision variables b 24 or c 25 must be examined next. Kraft, col. 6, lines 8-19.

Accordingly, Kraft shows that at least three branch decisions are needed to traverse the binary tree. These three branch decisions clearly exceed the "no more than two branch decisions" recited in claim 1. Accordingly, Kraft fails to teach or suggest "generating a plurality of minimum-degree polynomials based on no more than six equations having no more than two branch decisions." Oh, which is not relied upon to teach this feature, also fails to teach or suggest this feature of claim 1.

For at least the foregoing reasons, the cited art does not teach or suggest claim 1.

III. Whether claim 13 is unpatentable under 35 U.S.C. §103(a) over Oh in view of Kraft

Claim 13 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Oh in view of Kraft. FOA, p. 2. Claim 13 recites: "calculating a plurality of minimum-degree polynomials."

The Examiner cites col. 2, lines 43-51 and col. 6, lines 35-57 of Kraft as teaching calculating a plurality of minimum-degree polynomials. NFOA, page 5. However, the cited portion of col. 2 simply states:

> The error-location polynomial for a three-error correcting BCH code is a third order, or lower, polynomial whose coefficients belong to the field GF(2.sup.m). This polynomial's lowest order coefficient is 1, and its roots can be directly used to find the bits that are in error in the received codeword by well known methods. Mathematically, finding this polynomial consists of solving a system of non-linear equations over the Galois field or an equivalent simplification of this process.

This portion of Kraft simply describes the characteristics of the error-location polynomial as well as how the error-location polynomial can be found by solving a system of non-linear equations. It clearly neither teaches nor suggests "calculating a plurality of minimum-degree polynomials."

The cited portion of col. 6 of Kraft is presented above. As noted there, while Kraft's disclosure does show several polynomials (each identified by a respective one of temporary control bits *el*1-*el*8) in lines 37-47 of col. 6, multiple ones of these polynomials are not generated in the process of extracting an error polynomial. Instead, a

single one of those polynomials is selected as the error locator polynomial, based on which temporary control bit is identified by the traversal of the binary decision tree. Accordingly, Kraft does not teach or suggest calculating a plurality of minimum-degree polynomials, as recited in claim 13. As noted above with respect to claim 1, Oh also fails to teach or suggest this feature. For at least the foregoing reasons, the cited art does not teach or suggest claim 13.

IV. Whether claim claims 48 is unpatentable under 35 U.S.C. § 103(a) over Alvarez in view of Kraft

Claim 48 stands rejected as being unpatentable over Alvarez in view of Kraft, as indicated on p. 2 of FOA.

Claim 48 recites "wherein said decoding means uses a non-iterative algorithm to generate the error polynomial based on a plurality of minimum-degree polynomials." The rejection of this feature of claim 48 depends upon Kraft:

> Alvarez et al. do not explicitly teach... means for generating an error polynomial... based on a plurality of minimum-degree polynomials... Kraft in an analogous art teaches that the current invention teaches the non-iterative use of a decision-tree with closed formulas over the Galois field for the polynomial coeffecients (col. 4, lines 35-38, Kraft). Kraft also teaches that this invention teaches a combinatorial circuit with no clocks and no sequential operations (col. 4, lines 39-41 of Kraft). Kraft teaches that the object of the present invention... Galois Field GF (col. 4, lines 50-57, Kraft). Kraft teaches that the invention depicted in FIG. 1... more than three errors (fig. 1, 2, col. 6, lines 2-59, Kraft). NFOA, p. 17.

None of the teachings of Kraft cited above appear to contain any teaching or suggestion to generate an error polynomial based on a plurality of minimum-degree equations. The cited portions of col. 4 state:

> The current invention teaches the non-iterative use of a derision tree with closed formulas over the Galois Field for the polynomial coefficients. Prior art teaches the use of sequential circuits using many clock cycles; this invention teaches a combinational circuit with no clocks and no sequential operations. Kraft, col. 4, lines 35-41; and
>
> It is therefore the object of the present invention to provide a fast combinational decoder circuit capable of being realized as a VLSI device or a discrete circuit that converts the first three odd components of the

> syndrome vector of a three-error correcting (or less) binary BCH code into the three non-trivial coefficients of the error-location polynomial over the Galois Field GF(2^m). Kraft, col. 4, lines 50-57.

Thus, the above sections of Kraft clearly make no mention of or suggestion to generate an error polynomial based on a plurality of minimum-degree equations.

The portions of col. 6 cited in the rejection of claim 48 (which are discussed above in the rejection of claim 1) also fail to teach or suggest this feature of claim 48. As noted above with respect to claim 1, these portions of Kraft simply describe a technique for selecting one of several possible pre-generated error locator polynomials based upon the outcome of a binary decision tree traversal and do not teach or suggest generating an error polynomial based on minimum-degree polynomials.

Accordingly, the cited portions of Kraft do not teach or suggest generating an error polynomial based on a plurality of minimum-degree polynomials. The cited portions of Alvarez, which are not relied upon to teach this feature of claim 48, also fail to teach or suggest such a feature. For at least the foregoing reasons, the cited art does not teach or suggest claim 48.

CONCLUSION

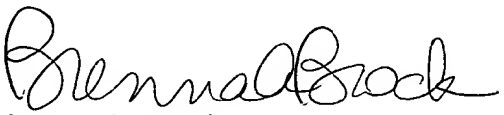
For the above reasons, Appellant respectfully submits that the rejections of pending claims 1-8, 10-29, 31-37, and 48-55 are unfounded. Accordingly, Appellant respectfully requests that the Board reverse the rejections of these claims.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop: Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA, 22313-1450, on November 3, 2006.

Attorney for Appellant

11/3/2006
Date of Signature

Respectfully submitted,



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CLAIMS APPENDIX

1. A method of decoding an error-correction code in a data signal, comprising the steps of:

receiving the data signal at a decoding unit;

computing a plurality of syndromes associated with the data signal using the decoding unit;

extracting an error polynomial from the data signal, wherein the extracting comprises generating a plurality of minimum-degree polynomials based on no more than six equations having no more than two branch decisions; and

locating errors within the data signal using the error polynomial.

2. The method of Claim 1 wherein said extracting step extracts the error polynomial in no more than 12 clock cycles.

3. The method of Claim 1 wherein said extracting step includes the step of controlling a plurality of Galois field multiply accumulators using a state machine.

4. The method of Claim 3 wherein each of the plurality of Galois field multiply accumulators represents a different power of the error polynomial.

5. The method of Claim 1 wherein said computing, extracting, and locating steps use a Bose-Chaudhuri-Hocquenghem (BCH) code.

6. The method of Claim 1 wherein said computing steps computes 2t syndromes, where t is a number of correctable errors which the error-correcting code can correct.

7. The method of Claim 1 wherein said computing step uses a linear feedback register to compute the syndromes.

8. The method of Claim 1 wherein said computing step includes the steps of:

dividing a received code word in the data signal by a minimal Galois polynomial; and

evaluating a remainder from said dividing step.

9. The method of Claim 1 wherein said extracting step generates the error polynomial based on the following six equations:

(1) $d_0 = S_1$,

(2) $d_1 = S_3 + S_1S_2$,

(3) $\sigma^1(X) = 1 + S_1X$,

(4) if $(d_1 = 0)$ then $\sigma^2(X) = \sigma^1(X)$

else if $(d_0 = 0)$ then $\sigma^2(X) = q_0\sigma^1(X) + d_1X^3$

else $\sigma^2(X) = q_0\sigma^1(X) + d_1X^2$,

(5) $d_2 = S_5\sigma_0 + S_4\sigma_1 + S_3\sigma_2 + S_2\sigma_3$, and

(6) if ($d_2 = 0$) then $\sigma^3(X) = \sigma^2(X)$

else $\sigma^3(X) = q_1\sigma^1(X) + d_1X^3$,

where S_i are the syndromes, σ^i are the minimum-degree polynomials, σ_i are four coefficients for $\sigma^2(X)$, d_0-d_2 are correction factors, q_0-q_1 are additional correction factors, q_0 is equal to d_0 unless d_0 is zero, when q_0 is 1, and q_1 is equal to d_1 unless d_1 is zero, when $q_1 = q_0$.

10. The method of Claim 1 wherein said extracting step includes the step of calculating correction terms using four Galois field multiply accumulators.

11. The method of Claim 1 wherein said locating step locates the errors by determining roots of the error polynomial which correspond to error locations.

12. The method of Claim 11 wherein said locating step uses Chien's algorithm to search for the error location numbers.

13. A method of determining an error polynomial for decoding a Bose-Chaudhuri-Hocquenghem (BCH) code, comprising the steps of:

computing a plurality of syndromes associated with a data signal having a BCH code embedded therein;

feeding the syndromes to a plurality of Galois field multiply accumulators;

calculating a plurality of minimum-degree polynomials associated with the BCH code, using the Galois field multiply accumulators; and

generating an error polynomial based on the minimum-degree polynomials, said calculating and generating steps extracting the error polynomial in no more than 12 clock cycles.

14. The method of Claim 13 wherein said calculating step includes the step of calculating a plurality of coefficients of at least one of the minimum-degree polynomials.

15. The method of Claim 13 wherein said calculating step includes the step of computing a first correction term using at least one of the Galois field multiply accumulators, the first correction term being equal to a first one of the syndromes.

16. The method of Claim 15 wherein said calculating step includes the step of computing a second correction term using at least one of the Galois field multiply accumulators, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes

17. The method of Claim 15 wherein said step of computing the first correction term includes the step of operating the at least one Galois field multiply accumulator in a pass-through mode.

18. The method of Claim 13 wherein:

the BCH code is a triple-error correcting code; and

said calculating step calculates at least three minimum-degree polynomials.

19. The method of Claim 18 wherein said calculating step further includes the steps of:

computing a first correction term using at least one of the Galois field multiply accumulators, the first correction term being equal to a first one of the syndromes;

computing a second correction term using at least one of the Galois field multiply accumulators, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes; and

computing a third correction term using at least one of the Galois field multiply accumulators, the third correction term being based in part on coefficients of at least one of the minimum-degree polynomials.

20. The method of Claim 19 wherein said calculating step includes the step of determining whether the second correction term is equal to zero.

21. The method of Claim 20 wherein said calculating step equates a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the second correction term is equal to zero.

22. The method of Claim 19 wherein said calculating step includes the step of determining whether the third correction term is equal to zero.

23. The method of Claim 22 wherein said calculating step equates a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the third correction term is equal to zero.

24. The method of Claim 18 wherein there are exactly four of the Galois field multiply accumulators, and said calculating step includes the step of controlling inputs to the Galois field multiply accumulators using a state machine.

25. A circuit for generating an error polynomial of a Bose-Chaudhuri-Hocquenghem (BCH) code, comprising:

a plurality of syndrome inputs;

a plurality of Galois field multiply accumulators; and

means for using said Galois field multiply accumulators to generate an error polynomial by generating a plurality of minimum-degree polynomials based on values provided at said syndrome inputs, by executing no more than six equations with two branch decisions.

26. The circuit of Claim 25 wherein said using means includes a state machine which asserts control ports on the Galois field multiply accumulators to execute the equations.

27. The circuit of Claim 25 wherein said using means computes a first correction term using at least one of the Galois field multiply accumulators, by assigning a value of a first one of the syndromes to the first correction term.

28. The circuit of Claim 27 wherein said using means further computes a second correction term using at least one of the Galois field multiply accumulators, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes.

29. The circuit of Claim 27 wherein said using means computes the first correction term by operating at least one Galois field multiply accumulator in a pass-through mode.

30. Canceled

31. The circuit of Claim 25 wherein said using means uses the Galois field multiply accumulators to calculate a plurality of coefficients of at least one of the minimum-degree polynomials.

32. The circuit of Claim 25 wherein:

the BCH code is a triple-error correcting code; and

said using means uses the Galois field multiply accumulators to calculate at least three minimum-degree polynomials.

33. The circuit of Claim 25 wherein said using means uses the Galois field multiply accumulators to:

compute a first correction term, by assigning a value of a first one of the syndromes to the first correction term;

compute a second correction term, the second correction term being equal to the sum of a product of the first syndrome with a second one of the syndromes, and a third one of the syndromes; and

compute a third correction term, the third correction term being based in part on coefficients of at least one of the minimum-degree polynomials.

34. The circuit of Claim 33 wherein said using means includes means for determining whether the second correction term is equal to zero.

35. The circuit of Claim 34 wherein said using means equates a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the second correction term is equal to zero.

36. The circuit of Claim 33 wherein said using means includes means for determining whether the third correction term is equal to zero.

37. The circuit of Claim 36 wherein said using means equates a first one of the minimum-degree polynomials to a second one of the minimum-degree polynomials in response to a determination that the third correction term is equal to zero.

38. A decoder circuit comprising:

a plurality of Galois field multiply accumulators; and

a state machine programmed to use said Galois field multiply accumulators to generate an error polynomial based on the following six equations:

(1) $d_0 = S_1$,

(2) $d_1 = S_3 + S_1S_2$,

(3) $\sigma^1(X) = 1 + S_1X$,

(4) if $(d_1 = 0)$ then $\sigma^2(X) = \sigma^1(X)$

else if $(d_0 = 0)$ then $\sigma^2(X) = q_0\sigma^1(X) + d_1X^3$

else $\sigma^2(X) = q_0\sigma^1(X) + d_1X^2$,

(5) $d_2 = S_5\sigma_0 + S_4\sigma_1 + S_3\sigma_2 + S_2\sigma_3$, and

(6) if $(d_2 = 0)$ then $\sigma^3(X) = \sigma^2(X)$

else $\sigma^3(X) = q_1\sigma^1(X) + d_1X^3$,

where S_i are error syndromes, σ^i are minimum-degree polynomials, σ_i are four coefficients for $\sigma^2(X)$, d_0-d_2 are correction factors, q_0-q_1 are additional correction factors, q_0 is equal to d_0 unless d_0 is zero, when q_0 is 1, and q_1 is equal to d_1 unless d_1 is zero, when $q_1 = q_0$.

39. The decoder circuit of Claim 38 wherein each of the Galois field multiply accumulators represents a different power of the error polynomial.

40. The decoder circuit of Claim 38 wherein said state machine is programmed to operate a selected one or more of said Galois field multiply accumulators in a pass-through mode.

41. The decoder circuit of Claim 38 wherein said state machine and said Galois field multiply accumulators are formed in a common application-specific integrated circuit.

42. The decoder circuit of Claim 38 wherein:

the BCH code is a triple-error correcting code; and

there are exactly four of said Galois field multiply accumulators.

43. The decoder circuit of Claim 42 wherein equation (1) is performed using a first one of said Galois field multiply accumulators.

44. The decoder circuit of Claim 43 wherein equation (2) is performed using said first Galois field multiply accumulator and a second one of said Galois field multiply accumulators.

45. The decoder circuit of Claim 44 wherein equation (3) is performed using said first and second Galois field multiply accumulators.

46. The decoder circuit of Claim 38 wherein:

at least one of said Galois field multiply accumulators has a first multiplexer whose output is coupled to a first input of a Galois field multiplier, a second multiplexer whose output is coupled to a second input of said Galois field multiplier, and a third multiplexer whose output is coupled to a first input of a Galois field adder, wherein an output of said Galois field multiplier is further coupled to a second input of said Galois field adder; and

said state machine controls respective select lines for each of said multiplexers.

47. The decoder circuit of Claim 46 further comprising means for determining when an output of said Galois field adder is equal to zero.

48. An OC-192 input/output card comprising:

four OC-48 processors; and

an OC-192 front-end application-specific integrated circuit (ASIC) connected to said four OC-48 processors, said OC-192 front-end ASIC having means for de-interleaving an OC-192 signal to create four OC-48 signals, and means for decoding error-correction codes embedded in each of the four OC-48 signals, said decoding means including means for generating an error polynomial associated with a given one of the error-correction codes in no more than 12 clock cycles, wherein said decoding means uses a non-iterative algorithm to generate the error polynomial based on a plurality of minimum-degree polynomials.

49. The OC-192 input/output card of Claim 48 wherein said decoding means includes a plurality of Galois field multiply accumulators.

50. The OC-192 input/output card of Claim 49 wherein said decoding means further includes a state machine controlling said Galois field multiply accumulators.

51. The OC-192 input/output card of Claim 49 wherein said decoding means uses said Galois field multiply accumulators to generate an error polynomial for a Bose-Chaudhuri-Hocquenghem (BCH) triple-error correcting code.

52. The OC-192 input/output card of Claim 51 wherein said decoding means includes no more than four of said Galois field multiply accumulators.

53. The OC-192 input/output card of Claim 51 wherein said decoding means includes means for computing a plurality of BCH syndromes which are used by said Galois field multiply accumulators to generate the error polynomial.

54. The OC-192 input/output card of Claim 48 wherein said decoding means locates errors within the data signal by applying Chien's algorithm to the error polynomial to search for error location numbers.

55. The method of claim 1, wherein said extracting comprises using a non-iterative algorithm to generate the error polynomial from the data signal based on no more than six equations having no more than two branch decisions.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None